IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listing, of claims in the application:

1-25 (Canceled).

26. (Previously presented) A method of manufacturing a wiring in a semiconductor device comprising the steps of:

forming a tungsten film by a sputtering method; and

patterning the tungsten film,

wherein an amount of sodium contained within the wiring is 0.3 ppm or less.

27. (Previously presented) The method according to claim 26, wherein the sputtering method uses a tungsten target having a purity of 4N or more.

28. (Previously presented) The method according to claim 26, wherein the sputtering method uses argon as a sputtering gas.

29. (Previously presented) The method according to claim 26, wherein the sputtering method is performed at a substrate temperature of 300 °C or lower.

30. (Previously presented) The method according to claim 26, wherein the sputtering method is performed at a gas pressure from 1.0 Pa to 3.0 Pa.

31. (Previously Presented) A method of manufacturing a semiconductor device having a gate electrode comprising the steps of:

forming a tungsten film by a sputtering method; and

patterning the tungsten film to form the gate electrode,

wherein an amount of sodium contained within the gate electrode is 0.3 ppm or less.

32. (Previously presented) The method according to claim 31, wherein the sputtering method uses a tungsten target having a purity of 4N or more.

33. (Previously presented) The method according to claim 31, wherein the sputtering method uses argon as a sputtering gas.

34. (Previously presented) The method according to claim 31, wherein the sputtering method is performed at a substrate temperature of 300 °C or lower.

35. (Previously presented) The method according to claim 31, wherein the sputtering method is performed at a gas pressure from 1.0 Pa to 3.0 Pa.

36. (Previously presented) A method of manufacturing a semiconductor device comprising the steps of:

forming a tungsten film by a sputtering method;

patterning the tungsten film to form a wiring; and

forming a semiconductor film over the wiring,

wherein an amount of sodium contained within the wiring is 0.3 ppm or less.

37. (Previously presented) The method according to claim 36, wherein the sputtering method uses a tungsten target having a purity of 4N or more.

38. (Previously presented) The method according to claim 36, wherein the sputtering method uses argon as a sputtering gas.

39. (Previously presented) The method according to claim 36, wherein the sputtering method is performed at a substrate temperature of 300 °C or lower.

40. (Previously presented) The method according to claim 36, wherein the sputtering method is performed at a gas pressure from 1.0 Pa to 3.0 Pa.

41. (Previously Presented) A method of manufacturing a semiconductor device having a gate electrode comprising the steps of:

forming a tungsten film by a sputtering method;

patterning the tungsten film to form a wiring to form the gate electrode; and

forming a semiconductor film over the wiring,

wherein an amount of sodium contained within the gate electrode is 0.3 ppm or less.

42. (Previously presented) The method according to claim 41, wherein the sputtering method uses a tungsten target having a purity of 4N or more.

43. (Previously presented) The method according to claim 41, wherein the sputtering method uses argon as a sputtering gas.

44. (Previously presented) The method according to claim 41, wherein the sputtering method is performed at a substrate temperature of 300 °C or lower.

45. (Previously presented) The method according to claim 41, wherein the sputtering method is performed at a gas pressure from 1.0 Pa to 3.0 Pa.

46. (New) The method according to claim 26, wherein a stress of the wiring is within a range of from -5×10^{10} to 5×10^{10} dyn/cm^2.

47. (New) The method according to claim 31, wherein a stress of the gate electrode is within a range of from -5×10^{10} to 5×10^{10} dyn/cm^2.

48. (New) The method according to claim 36, wherein a stress of the wiring is within a range of from -5×10^{10} to 5×10^{10} dyn/cm^2.

49. (New) The method according to claim 41, wherein a stress of the gate electrode is within a range of from -5×10^{10} to 5×10^{10} dyn/cm^2.